WHAT IS CLAIMED IS:

1. An instruction decompressor configured to decompress compressed instructions, wherein a first one of said compressed instructions is codable to access a first subset of registers defined for a corresponding non-compressed instruction set, and wherein a second one of said compressed instructions is codable to access said first subset of registers and is further codable to access a second subset of registers.

2. The instruction decompressor as recited in claim 1 wherein said second one of said compressed instructions is assigned a first opcode encoding and a second opcode encoding.

3. The instruction decompressor as recited in claim 2 wherein said first opcode encoding indicates that said second one of said compressed instructions is coded to access one of said first subset of registers.

4. The instruction decompressor as recited in claim 3 wherein said instruction decompressor decompresses said second one of said compressed instructions using a first mapping of compressed register codings to decompressed register codings, wherein said first mapping maps each compressed register coding to a decompressed register coding within said first subset.

5. The instruction decompressor as recited in claim 4 wherein said second opcode encoding indicates that said second one of said compressed instructions is coded to

access one of said second subset of registers.

6. The instruction decompressor as recited in claim 5 wherein said instruction decompressor decompresses said second one of said compressed instructions using a second mapping of compressed register codings to decompressed register codings, wherein said second mapping maps each of said compressed register codings to a decompressed register coding within said second subset of registers.

7. The instruction decompressor as recited in claim 2 wherein said second one of said compressed instructions includes a first register field and a second register field.

8. The instruction decompressor as recited in claim 7 wherein said instruction decompressor decompresses said first register field according to said first subset of registers if said first opcode encoding is used.

9. The instruction decompressor as recited in claim 8 wherein said instruction decompressor decompresses said first register field according to said second subset of registers if said second opcode encoding is used.

10. The instruction decompressor as recited in claim 9 wherein said second one of said compressed instructions is assigned a third opcode encoding, wherein said decompressor decompresses said second register field using said second subset of registers if said third opcode encoding is used.

11. The instruction decompressor as recited in claim 10 wherein said second one of said compressed instructions is

assigned a fourth opcode encoding, wherein said decompressor decompresses said first register field and said second register field using said second subset of registers if said fourth opcode encoding is used.

12. The instruction decompressor as recited in claim 2 wherein said first opcode encoding and said second opcode encoding differ in bits included in a function field of said second one of said compressed instructions.

13. A method for decompressing compressed instructions, comprising:

decompressing a particular compressed instruction having a first register field using a first register mapping from compressed register indicators to decompressed register indicators for decompressing said first register field if said particular compressed instruction is encoded using a first opcode; and

decompressing said particular compressed instruction having said first register field using a second register mapping from compressed register indicators to decompressed register indicators for decompressing said first register field if said particular compressed instruction is encoded using a second opcode.

14. The method as recited in claim 13 wherein said particular compressed instruction further includes a second register field.

15. The method as recited in claim 14 further comprising decompressing said second register field using said second register mapping if said particular compressed instruction is encoded using a third opcode.

16. The method as recited in claim 15 further comprising decompressing said second register field and said first register field using said second register mapping if said particular compressed instruction is encoded using a fourth opcode.

17. The method as recited in claim 13 further comprising decompressing a second particular compressed instruction using said first mapping.

18. The method as recited in claim 17 wherein said second particular compressed instruction includes one opcode encoding.

19. An apparatus for decompressing compressed instructions comprising a decompressing means, wherein said decompressing means is configured to decompress a particular compressed instruction having a first register field using a first register mapping from compressed register indicators to decompressed register indicators for decompressing said first register field if said particular compressed instruction is encoded using a first opcode, and wherein said decompressing means is further configured to decompress said particular compressed instruction having said first register field using a second register mapping from compressed register indicators to decompressed register

indicators for decompressing said first register field if said particular compressed instruction is encoded using a second opcode.

20. An instruction decompressor configured to decompress a compressed register field of a compressed instruction into a decompressed register field of a decompressed instruction, wherein a decompression of said compressed register field is dependent upon a first value coded into said compressed register field and a second value coded into an opcode field of said compressed instruction.

21. The instruction decompressor as recited in claim 20 wherein said instruction decompressor is configured to select one of multiple mappings from compressed register field encodings to decompressed register field encodings in response to said second value.

22. The instruction decompressor as recited in claim 21 wherein said instruction decompressor selects one of said decompressed register encodings from said one of said multiple mappings in response to said first value.

23. The instruction decompressor as recited in claim 22 wherein a particular instruction is assigned a first opcode encoding and a second opcode encoding, and wherein said instruction decompressor, upon receipt of said particular instruction having said first opcode encoding selects said one of said multiple mappings for decompressing said compressed register field.

24. The instruction decompressor as recited in claim 23 wherein said instruction decompressor, upon receipt of said particular instruction having said second opcode encoding selects another one of said multiple mappings for decompressing said compressed register field.

25. A method for decompressing a compressed register field of a compressed instruction into a decompressed register field of a decompressed instruction, comprising:

directly copying at least a portion of said compressed register field into a portion of said decompressed register field; and

logically operating upon said compressed register field to produce a remaining portion of said decompressed register field.

26. The method as recited in claim 25 wherein said portion of said compressed register field comprises an entirety of said compressed register field.

27. The method as recited in claim 26 wherein said portion of said decompressed register field receiving said entirety of said compressed register field comprises a plurality of least significant bits of said decompressed register field.

28. The method as recited in claim 27 wherein said plurality of least significant bits is equal in number to a number of bits comprising said compressed instruction field.

29. The method as recited in claim 25 further comprising logically operating upon an opcode field of said compressed instruction to produce said remaining portion of said decompressed register field.

30. The method as recited in claim 29 wherein said logically operating upon said opcode field comprises selecting a first register mapping in response to a first opcode encoding in said opcode field.

31. The method as recited in claim 30 wherein said logically operating upon said opcode field further comprises selecting a second register mapping in response to a second opcode encoding in said opcode field.

32. The method as recited in claim 31 wherein said first opcode encoding and said second opcode encoding are assigned to a particular instruction.

33. An apparatus for decompressing a compressed register field of a compressed instruction into a decompressed register field of a decompressed instruction, comprising:

a first means for directly copying at least a portion of said compressed register field into a portion of said decompressed register field, wherein said first means is coupled to receive said compressed register field; and

a second means for logically operating upon said compressed register field to produce a remaining portion of said decompressed register field,

wherein said second means is coupled to receive said compressed register field.

34. The apparatus as recited in claim 33 wherein said portion of said compressed register field comprises an entirety of said compressed register field.

35. The method as recited in claim 34 wherein said portion of said decompressed register field receiving said entirety of said compressed register field comprises a plurality of least significant bits of said decompressed register field.

36. An instruction decompressor configured to decompress a compressed register field of a compressed instruction into a decompressed register field of a decompressed instruction, wherein said instruction decompressor forms a first portion of said decompressed register field by copying at least a portion of said compressed register field thereto, and wherein said instruction decompressor includes a logic block which is configured to operate upon said compressed register field to produce a remaining portion of said decompressed register field.

37. The instruction decompressor as recited in claim 36 wherein said portion of said compressed register field comprises an entirety of said compressed register field.

38. The instruction decompressor as recited in claim 36 wherein said logic block selects a register mapping from compressed register field encodings to decompressed register field encodings in response to a signal received from said instruction decompressor.

39. The instruction decompressor as recited in claim 38 wherein said instruction decompressor is configured to assert said signal upon detection of a first opcode assigned to a particular instruction, and wherein said instruction decompressor is configured to deassert said signal upon detection of a second opcode assigned to said particular instruction.

40. The instruction decompressor as recited in claim 36 wherein said portion of said decompressed register field receiving said portion of said compressed register field comprises a plurality of least significant bits of said decompressed register field.

41. The instruction decompressor as recited in claim 40 wherein said plurality of least significant bits are equal in number to a number of bits comprising said compressed register field.